27.6 A DLL with Jitter-Reduction Techniques for DRAM Interfaces

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Recently, demand has grown for high-bandwidth DRAMs to address high-capacity multimedia applications. A delay-locked loop (DLL) is a key component for achieving better timing margin in DRAM interfaces. A replica delay line in the DLL is susceptible to supply noise originating from switching noise in the DRAM core. Many solutions have been reported to improve the jitter performance of high-frequency clock under noisy environments [1,2]. This paper presents a jitter-immune DLL that suppresses the delay variation induced by the jitter of the replica delay line. The jitter reduction techniques control the loop behavior by monitoring the amount of jitter to optimize the jitter tolerance. This design also introduces a new architecture to generate I/Q phase, which has a wide operating range.

Figure 27.6.1 shows the quadrature phase generation loop (QPGL). A differential input signal of 50% duty is needed to generate accurate Q and I phases. A differential pulse adjuster outputs two single-ended signals (DPA_p, DPA_n) with variable pulse width. The Q signal goes high at the rising edge of the DPA_p, and low at the rising edge of the DPA_n. The I signal becomes high at the falling edge of the DPA_p, and low at the falling edge of the DPA_n. The phase difference between Q and I is maintained at 90º through the feedback operation of the loop. The QPGL allows both coarse tuning and fine tuning. Coarse tuning selects an adequate range for the input frequency so that precise Q and I phases are produced in the fine tuning. When the V_C exceeds the upper limit (V_H) or the lower limit (V_L), the range-selection unit changes the range and resets the V_C to $V_{DD}/2$. In the graph showing the operating frequency versus V_C, four fine tuning ranges overlap each other for the continuity of total tuning range. The QPGL achieves low jitter over a wide operating range because of lower gain in the fine tuning and the range switching by the coarse tuning.

Figure 27.6.2 shows the structure of the differential pulse adjuster. The analog control voltage (V_C) is for the fine tuning and digital control bits (EN0, EN1) are for the coarse tuning. The falling transition by NMOS (MN1, MN2) is fast enough, and it is invulnerable to V_C variation. On the other hand, the slope of the rising transition decreases as V_C increases, because the resistance of MN3 and MN4 varies the amount of effective gate capacitance of MP1 and MP2 seen by the output node. As a result, the output signal has variable pulse width according to the value of the V_C. The minimum value of the V_C is above the threshold voltage of NMOS to prevent a lasting floating state at the PMOS gate node. Since the QPGL monitors the value of V_C to select the operating range, the range of the V_C has an upper and the lower limit that covers the threshold voltage limit.

Figure 27.6.3 shows the block diagram of the proposed DLL. The duty cycle corrector (DCC) removes the duty distortion of the input. The QPGL generates the Q and I signal as well as digital bits (EN0, EN1) that define the adequate operating range according to the clock frequency. The main loop generates the output clock (CLK_{OUT}) by interpolating four phases (Q, I, /Q, /I). For the smooth output transition of the phase interpolator (PI) over a wide range [3], the input slew rate of the PI is adjusted by digital bits (EN0, EN1), which are generated in the QPGL. The main loop introduces a masking window control scheme to suppress the jitter due to the supply noise of the replica delay line. The jitter, whose magnitude is less than the window size, is neglected in the loop by disabling the charge pump (CP), and the loop has no reaction. When the jitter magnitude is beyond the window size, the LOCK signal is disabled and the loop tracks the phase error. If the window size is wide, the CLK_{OUT} has less jitter by reducing the quantity of unnecessary loop response against the dirty jitter of the clock from the replica delay line (CLK_{RDL}). However, the loop cannot track the small phase error which may result from incomplete locking and minor variation of V_C due to the leakage. To reach a balance between the jitter suppression extent and the phase error tracking, the window size is adjusted according to the amount of jitter in the replica delay line.

Figure 27.6.4 illustrates the masking window control loop (MWCL), which uses the pulse reshaper of [4]. In the charge pump (CP_{MWC}), I_{UP} is four times larger than I_{DN}. When the phase difference is within the window, the LOCK signal goes high and the window size decreases at the rate of α. However, if the phase difference exceeds the window, the LOCK signal becomes low and window size increases at the rate of 4α. To simplify the design analysis, we assume that the jitter of the CLK_{RDL} has a uniform probability density function. The average current ($I_{average}$) of the CP_{MWC} is given by

$$I_{average}=I_{UP}\times P_{Unlock}-I_{DN}\times P_{Lock}=4I_{DN}\times(J_{PP}-W)/J_{PP}-I_{DN}\times W/J_{PP},$$

where P_{Lock} is the probability of the locked state, P_{Unlock} is the probability of the unlocked state, W is the window size, and J_{PP} is the peak-to-peak jitter of the CLK_{RDL}. As $I_{average}$ becomes zero, the window size converges into $4/5\times J_{PP}$. The main loop controls its loop behavior with a hysteresis of two cycles of the LOCK signal to suppress high frequency noise with large magnitude. Although the main loop maintains the stable behavior of a first-order system, its tracking bandwidth is above the loop bandwidth of the MWCL to prevent under-damped behavior of window convergence. However, if the loop bandwidth of the MWCL is too low, it takes a long time for window convergence with an over-damped behavior. The masking window control voltage (V_{MWC}) is varied by $Pulse_{Lock}$ and $Pulse_{Unlock}$ whose pulses have a fixed width and are activated by the rising edge of the reference clock. As a result, the MWCL has critically damped behavior for window convergence over a wide operating range because it and the main loop have loop bandwidths proportional to the reference clock frequency.

A testchip is fabricated in a 0.13μm CMOS logic process. The replica delay line in the testchip is designed to have a noisy supply by eliminating its decoupling capacitors. We suppose that its internal switching noise is similar to real DRAM noise, which includes large switching noise when the DRAM core operates. To exhibit further jitter reduction effect, an external 400MHz sinusoidal signal of 6dBm is added to the supply of the replica delay line. Figure 27.6.5 shows the jitter histograms of the output clock when the masking window control function is ON and OFF. In the OFF condition, the main loop always tracks the phase error without disabling the CP. As a result, the noisy replica delay line makes the loop response busy, incurring the degradation of jitter performance. However, in the ON condition, the DLL has a low jitter output clock, which is tolerant of the jitter of the replica delay line. A die micrograph is shown in Fig. 27.6.6. Excluding the replica delay line and output buffers, the DLL consumes 6mW from a 1.2V supply.

References:

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[4] B.-G.. Kim and L.-S. Kim, "A 250-MHz-2-GHz Wide-Range Delay-Locked Loop," *IEEE J. Solid-State Circuits*, vol. 40, no. 40, pp. 1310-1321, Jun., 2005.

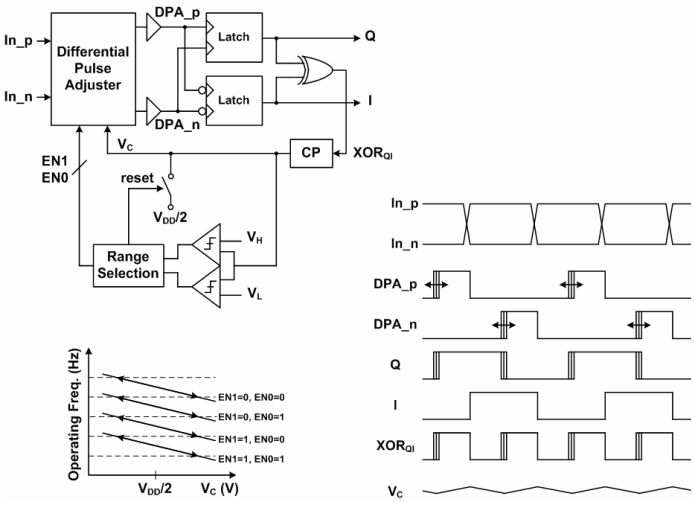


Figure 27.6.1: Architecture and timing diagram of quadrature phase generation loop.

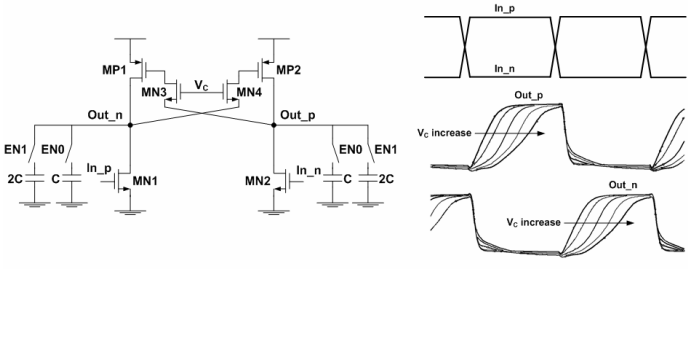


Figure 27.6.2: Structure and timing diagram of differential pulse adjuster.

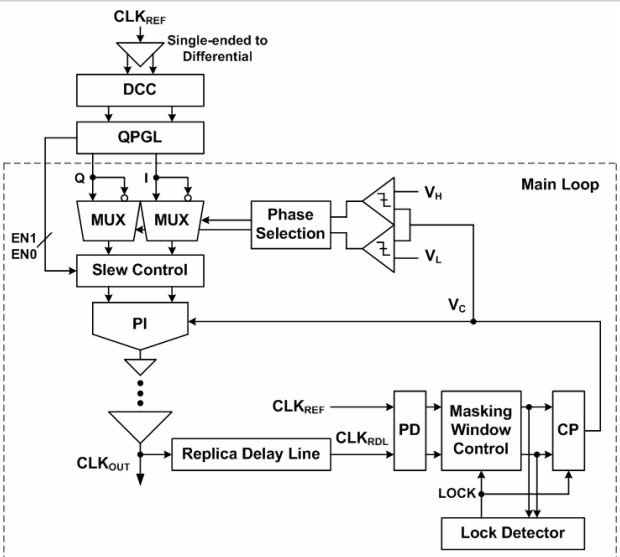


Figure 27.6.3: Block diagram of DLL.

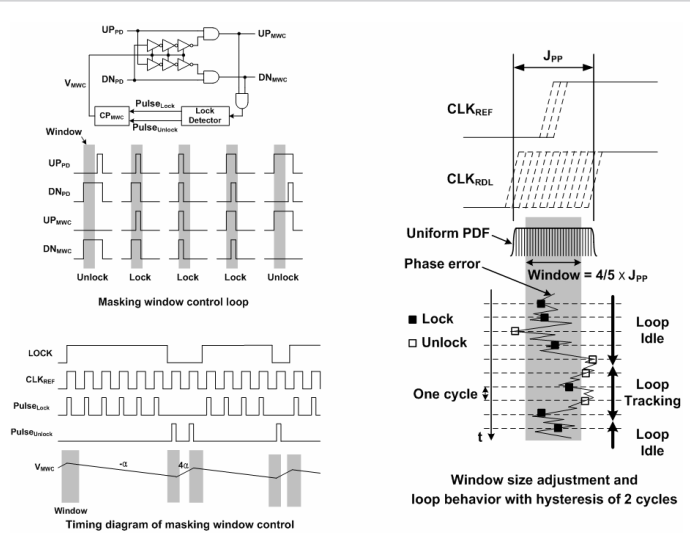
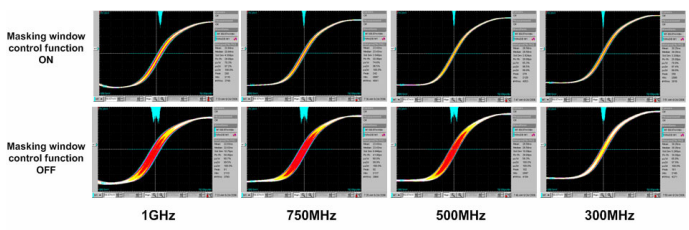
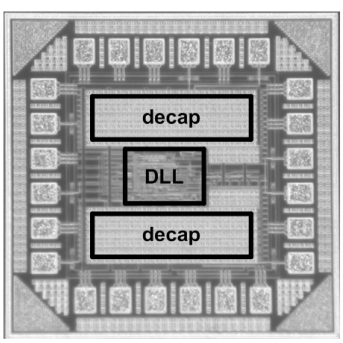


Figure 27.6.4: Masking window control scheme.



	1GHz		750MHz		500MHz		300MHz	
	rms	p-p	rms	p-p	rms	p-p	rms	p-p
Masking window control function ON	**4.58ps**	**29ps**	**3.54ps**	**22ps**	**2.92ps**	**20ps**	**3.21ps**	**25ps**
Masking window control function OFF	10.75ps	50ps	9.95ps	41ps	10.09ps	38ps	5.27ps	30ps

Figure 27.6.5: Jitter histograms of output clock.



Technology	0.13μm CMOS logic
Supply voltage	1.2V
Operating range	300MHz – 1GHz
Active area	250μm×150μm
Power consumption	6mW

Figure 27.6.6: Die micrograph.